**Independent Study Project**

Design and Implementation of an FPGA

**Project Description**

In this project the candidate will use a standard integrated circuit design flow for the design and implementation of a field programmable gate array integrated circuit (FPGA IC) in the GlobalFoundries 0.13um 8RF-DM process. The candidate will be required to build several components:

* SRAM architecture for chip programming
* SRAM programmable FPGA look-up table (LUT)
* Synchronous/Asynchronous D-FF
* SRAM programmable switch multiplexer
* Construction of a repeatable FPGA tile
* Integration of a final FPGA with the repeatable TILE

The final integrated circuit has a high likelihood of being fabricated for testing. The candidate will be expected to conduct independent research and study to fill any gaps in knowledge to achieve final integration though the supervisor will provide direction in where to look.

**Required Skills**

To be successful in this role, the candidate must be intimately familiar with digital logic design at the gate/transistor level and have a nominal understanding of mixed-signal transistor level circuit design.

The design flow involves several highly specialized skills:

* Transistor level schematic capture in MicroMagic SUE.
* Chip transistor and metal layer layout in MicroMagic MAX.
* Design rule checking (DRC) with Mentor Graphics Calibre nmDRC.
* Layout versus schematic (LVS) checking with Mentor Graphics Calibre LVS.
* Extraction of parasitic resistance and capacitance with Mentor Graphics Calibre xRC.
* SPICE simulation of circuits with layout parasitics with Mentor Graphics ELDO.

The candidate is expected to have knowledge of each task in the design flow, though experience with the individual tools by MicroMagic and Mentor Graphics are not required.